SPECIFICATION

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THINNING OF FUSE PASSIVATION AFTER C4 FORMATION

Background of Invention

[0001] *Technical Field*

[0002] The present invention relates generally to integrated circuits having fuse elements. More particularly, the present invention relates to a method of forming a fuse structure, and to a laser fuse deletion process.

[0003] *Related Art*

[0004] Laser fusing processes are typically used to delete specific fuses formed within integrated circuits. For example, laser-blown fuses are commonly used to repair defective regions on a chip. In such processes, one approach is to fabricate the fuse in the final metal layer of a multi-layer metallization structure, with one or more overlying layers of passivating material, such as silicon oxide or silicon nitride. Thereover, a final passivating layer, usually including polyimide, is formed, and an opening is made in the final passivating layer above the fuse. During the deletion process, the fuse is exposed to a laser pulse, which heats the metal fuse above its boiling point. The subsequent volume expansion cracks the passivating material over the fuse, so that it is substantially removed allowing the metal fuse to evaporate.

[0005] In forming a multilayer metallization structure, relatively new materials are starting to be used as one or more of the dielectric layers. These materials are low-k, i.e. with dielectric constants less than about 3.5, and are generally organic as well as porous, having much lower thermal and mechanical stability as compared to conventionally used materials, such as undoped and doped silicon oxide. Because of

these characteristics, these materials are not generally satisfactory as the dielectric for the final metal layer in which the fuse is fabricated, as damage to adjacent structures can result during the laser fuse deletion process. Consequently, it is generally preferable to use conventional dielectric materials for the final metal layer. Even so, damage can still occur to underlying low-k dielectric layers, due to their low thermal and mechanical stability. Therefore, in those structures in which such low-k dielectric materials are employed, the energy used in the laser fuse deletion process must be greatly reduced from that typically used for integrated circuits containing only conventional dielectric materials.

[0006] On the other hand, with a lower energy process, there is an increased risk of residual passivating material remaining over the fuse, i.e. the energy is insufficient to satisfactorily remove the passivating material. Accordingly, in such a process, the passivating material over the fuse should be as thin as possible, although thick enough to ensure that there is no oxidation or contamination of unblown fuses due to exposure to the ambient.

[0007] Also impacting the thickness of the passivating material over the fuse is the process of forming a controlled, collapse chip connection (C4) structure. A typical C4 process includes sputter cleaning and TiW etch steps tht will also reduce the thickness of the passivating material over the fuse, which can be on the order of about 100 nm, further hampering from attaining satisfactory thickness.

[0008] Therefore, there exists a need in the industry for an improved method of forming a fuse, and performing a laser deletion process, which includes effective integration with forming a C4 metallurgy structure.

Summary of Invention

[0009] It is against this background that the present invention provides a method of forming a fuse structure, according to which the passivating material over the fuse has a substantially uniform thickness, that is provided after forming a C4 metallurgy structure. The method is particularly suitable for multilevel-metallization structures which include low-k dielectric materials.

[0010] In accordance with the invention, there is provided a method of forming a fuse

structure, comprising: providing a substrate which comprises a C4 metallurgy contact pad and a fuse therein; forming an etch resistant layer over the C4 metallurgy contact pad and the fuse; forming at least one passivating layer over the etch resistant layer; removing at least a first portion of the at least one pasivating layer and the etch resistant layer to expose the C4 metallurgy contact pad; forming a C4 metallurgy structure on the C4 metallurgy contact pad; and thereafter removing at least a second portion of the at least one passivating layer to expose the etch resistant layer over the fuse.

[0011] Further, in accordance with the invention, there is provided a method of performing a fuse deletion process, comprising: providing a substrate which comprises a C4 metallurgy contact pad and a fuse therein; forming an etch resistant layer over the C4 metallurgy contact pad and the fuse; forming at least one passivating layer over the etch resistant layer; removing at least a first portion of the at least one passivating layer and the etch resistant layer to expose the C4 metallurgy contact pad; forming a C4 metallurgy structure on the C4 metallurgy contact pad; thereafter removing at least a second portion of the at least one passivating layer to expose the etch resistant layer over the fuse; and applying a radiant energy source to the fuse until the etch resistant layer over the fuse is substantially removed.

[0012] The foregoing and other features and advantages of the invention will be apparent from the following more particular description of embodiments of the invention.

Brief Description of Drawings

[0013] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:Figs. A-C are schematic section views illustrating the method in accordance with the present invention.

Detailed Description

[0014] Referring to the drawings, and more particularly to Fig. 1A, there is shown a cross-section of a substrate 1 having several metal wiring layers formed therein. In this embodiment, the substrate 1 is illustrated with three metal wiring layers, with each having metals 2-4 embedded in respective dielectric layers 5-7. It will be

understood, however, that greater or less than, three metal wiring layers, may be used in accordance with the invention. It is preferred that the final two dielectric layers 6 and 7 comprise a conventional dielectric material, such as silicon oxide or doped silicon oxide, e.g. fluorosilicate glass, to provide thermal and mechanical stability, although this is not required. However, the other dielectric layers may comprise either a conventional dielectric material or a low-k dielectric material (i.e., with a dielectric constant less than about 3.5), such as disclosed in U.S. Pat. No. 5,965,679, the entire contents of which are incorporated herein by reference. It is also preferred that metals 2-4 comprise copper, although other materials known to those skilled in the art can be employed. At least one region of the final metal wiring layer 4 forms a fuse 4A.

[0015] A plurality of passivating layers 8, 9 and 10 are deposited on the surface of the final metal wiring layer of the substrate 1. While silicon nitride, silicon oxide and silicon nitride are utilized in layers 8, 9, and 10, respectively, those skilled in the art will understand that other appropriate materials can be used. Standard photoresist and etch techniques are employed to form an opening 11 in the passivating layers 8, 9, and 10, where a C4 metallurgy structure is to be formed. A suitable material such as aluminum, titanium-tungsten, etc., is deposited in the opening 11 and etched to form a contact structure 12 on a contact pad 4 of the final metal wiring layer 4. A final layer of passivation 13, usually polyimide, is applied over the passivating layer 10 and the contact structure 12. By again using standard photoresist and etch techniques, a C4 window 14 above the contact structure 12 and a fuse window 15 above the fuse 4A are formed in the final layer of passivation 13.

[0016] Next, a C4 metallurgy structure is formed, as shown in Fig. 1B. After carrying out a sputter cleaning process of the contact structure 12 in the C4 window 14, barrier layer metallurgy (BLM) 15 is deposited and etched, using conventional techniques. Typically, titanium-tungsten is used for the BLM. Then, the C4 metallurgy 16 comprising, for example, lead and tin, is deposited, again using standard techniques such as electroplating or, alternatively, evaporation, etc., on the remaining BLM 15.

[0017]

Referring to Fig. 1C, dry RIE techniques, usually fluorine-based, are used to etch passivating layer 10 selectively to passivating layer 9, i.e. silicon nitride selectively to silicon oxide in this example, above the fuse 4A. Additionally, passivating layer 9 is

etched selectively to passivating layer 8, using dry RIE techniques, such as C4F8 or CHF3-based etch chemistries, to achieve high selectivity of silicon oxide to silicon nitride. It is important to control the etch of passivating layer 9 to passivating layer 8 above the fuse 4A so that it is thick enough, greater than about 75 nm for this example, to ensure that there is no oxidation or contamination of the unblown fuse 4A due to exposure to the ambient. However, at the same time, the remaining passivating layer 8 over the fuse 4A should be as thin as possible, yet ensure that low energy fuse blow is possible, which in this example would be less than about 150 nm. For manufacturing efficiency, it should be noted that these two etches can be combined with the BLM etch.

[0018] To eliminate or reduce potential contamination from these etch steps, it may be desirable to perform additional cleaning of the C4 metallurgy 16 and the surface of the final layer of passivation 13. Otherwise, contamination may degrade adhesion between the C4 metallurgy 16 and the package (not shown). As examples, an oxygen-ashing or sputter cleaning can be used to clean the surface of polyimide, and a hydrogen reflow anneal can be used to clean the surface of the C4 metallurgy 16, especially if there is oxidation of the surface from an oxygen-ashing process.

[0019] Further, in accordance with the method of the invention, it should be emphasized that the passivating layers 9 and 10 over the fuse 4A are etched after the C4 metallurgy 16 is formed. Otherwise, steps which are carried out during the C4 process, such as sputter cleaning and the BLM 15 etch, will also etch the passivating layer 8 over the fuse 4A. In practice, these C4 process steps can etch the passivating layer 8 by varying amounts, but as much as about 100 nm or more would be possible. Such variation would make it difficult to achieve the desired thickness of passivating layer 8 over the fuse 4A. By etching passivating layers 9 and 10 over the fuse 4A after C4 metallurgy 4 formation, the variability in passivating layer 8 thickness is greatly reduced.

[0020] The resulting fuse structure is shown in Fig. 1C, which is now ready for fuse blow. Further in accordance with the invention, a laser deletion process is performed to open the fuse 4A. In particular, a radiant energy source is applied to the fuse 4A until the passivating layer 8 over the fuse 4A is substantially removed. In a particularly

preferred embodiment, an infra-red laser emits a beam, with specified amount of energy, through the remaining thickness of the passivating layer 8 over the fuse 4A and into the fuse 4A. As the laser beam interacts with the fuse 4A material, the fuse 4A heats up and expands, so as to cause the passivating layer 8 over the fuse 4A to rupture. Following rupture, the molten metal of fuse 4A vaporizes so that fuse delete occurs.

[0021] While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. For example, it is important that the passivating layer 8 has a slower etch rate than the passivating layer 9 deposited over it, so that it provides etch resistant or etch stop characteristics, but other materials than those described can be used as long as these characteristics are provided. Similarly, although metals 2-4 are copper in the described embodiments, it is not necessary to use the same metal for all metal wiring layers, nor to necessarily use copper, although it is preferred. In addition, a wide variety of etch techniques, both dry and wet, and cleaning techniques, can be employed so that these steps are in no way limited to only those described. Also, although the metal wiring layers are preferably formed using damascene processing, other types of processing can be employed. Also, as previously noted, the invention is not limited to the specific number of layers shown. For example, the number of metal wiring layers or the number of passivating layers above the final wiring layer may be greater or less than those shown, and so forth. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.

[0022]